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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/733,844	12/11/2003	Michel Gillet	944-001.123	9020

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EXAMINER
PHAN, RAYMOND NGAN

ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 04/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

Office Action Summary	Application No.	Applicant(s)	
	10/733,844	GILLET, MICHEL	
	Examiner	Art Unit	
	Raymond Phan	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 February 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Part III DETAILED ACTION

Notice to Applicant(s)

1. This action is responsive to the following communications: remarks filed on Feb 3, 2006

2. This application has been examined. Claims 1-31 are pending.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-31 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Moro (US Pub No. 2003/0056050) in view of Iida et al. (US Pub No. 2004/0156242).

In regard to claims 1, 13, 22, 27, 30, Moro discloses a method for enhancing performance of an electronic device having a host module operatively connected to a memory device (i.e. SD card) via a bus system (see figure 6), the bus system comprising a plurality of signal lines and N data lines for conveying signals and data between the host module and the memory device (see figure 6, para. 0057), wherein the host module is operable in a plurality of data modes (i.e. SPI, SD-4), the plurality of modes including at least one data mode (i.e. SPI and/or SD-1) that use M data lines to convey data between the host module and the memory device, with M smaller than N (N-M) unused data lines in the bus system (see figure 6, paras 0055-0059), the method comprising the step of providing in the memory device a module for generating at least one further signal (see figure 6, paras. 55-

57). But Moro does not specifically disclose the step of causing to exchange of data, based on the at least one further signal, between the host module and the memory device using at least one of unused data lines even when the host module is operated in the at least one data mode. However Iida et al. disclose the step of causing to exchange of data, based on the at least one further signal, between the host module and the memory device using at least one of unused data lines even when the host module is operated in the at least one data mode (see figure 2, table 1, paras. 0041-0045). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Iida et al. into the teachings of Moro because it would provide technology to realize high speed data transfer while compatibility in a card type storage device.

In regard to claims 2, 15, 24, 28, Moro discloses wherein the further signal comprising a command signal, conveyed to the host module on another one of unused data lines (see figure 6, para 0055).

In regard to claims 3, 16, 23, 29, Moro discloses wherein the further signal comprising a clock signal, conveyed to the host module on another one of unused data lines (see figure 6, para 0055).

In regard to claim 4, Iida et al. disclose wherein N is equal to 8 (DAT0-DAT7) and M is equal to 4 (DAT0-DAT3), leaving 4 unused data line (see figure 2, table 1, paras 0041-0045), and wherein at least one further signal comprising a clock signal conveyed from the memory device to the host module on another one of the unused data lines, and a command signal, conveyed between the host module and the memory device on yet another one of the unused data lines (see figures 2, paras 0045-0049). Therefore, it would have been obvious to a person of

an ordinary skill in the art at the time the invention was made to have combined the teachings of Iida et al. into the teachings of Moro because it would provide technology to realize high speed data transfer while compatibility in a card type storage device.

In regard to claim 5, Moro discloses wherein at least one of the unused data lines comprising two unused data line for carrying out the exchange of data in a differential manner (see figures 2, table 1, paras 0041-0045).

In regard to claims 6, 19, 31, Moro discloses wherein the electronic device is operable in a serial peripheral interface (SPI) mode (see figure 5) and the bus system further comprising a further signal line for conveying a chip select (CS) signal from the host module to the memory device and wherein further signal is conveyed from the memory device to the host module on the further signal line (see figure 5-6, paras 0055-0057).

In regard to claims 7, 20, Moro discloses the further signal comprising a command signal (see figure 5).

In regard to claims 8, Iida et al. disclose wherein N is equal to 8 (DAT0-DAT7) and M is equal to 4 (DAT0-DAT3), leaving 4 unused data line (see figure 2, table 1, paras 0041-0045). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Iida et al. into the teachings of Moro because it would provide technology to realize high speed data transfer while compatibility in a card type storage device.

In regard to claims 9, 11, Iida et al. disclose wherein exchange of data is carried out in two differential pairs (see figure 2, table 1, paras. 0041-0045).

In regard to claim 10, Iida et al. disclose wherein N is equal to 8 (DAT0-DAT7) and M is equal to 4 (DAT0-DAT3), leaving 4 unused data line (see figure 2, table 1, paras 0041-0045), and wherein at least one further signal comprising a clock signal conveyed from the memory device to the host module on another one of the unused data lines, and a command signal, conveyed between the host module and the memory device on yet another one of the unused data lines (see figures 2, paras 0045-0049). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Iida et al. into the teachings of Moro because it would provide technology to realize high speed data transfer while compatibility in a card type storage device.

In regards to claim 12, Iida et al. disclose wherein exchange of data is carried out on two or more different unused data line (see figures 2, table 1, paras 0041-0045). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Iida et al. into the teachings of Moro because it would provide technology to realize high speed data transfer while compatibility in a card type storage device.

In regard to claim 14, Moro discloses wherein the memory device comprising an embedded module 14 for generating the at least one signal (see figure 2, paras 0039-0040).

In regard to claim 17, Moro discloses wherein the electronic device is a mobile phone (see para 0005).

In regard to claim 18, Moro discloses wherein the electronic device is a PDA (see para 0005).

In regard to claim 21, Moro discloses the program (see paras 0039-0040), responsive to the further signal, for processing the data exchanged between the host module and the memory device on at least one of the unused data lines (see para 0040).

In regard to claims 25-26, Moro discloses the module for generating at least further signal comprising a micro-controller or input/output device 14 (see figure 2, paras 0039-0040).

Response to Arguments

5. In view of remark filed on Feb 3, 2006, claims 1-31 have been fully considered but they are not deemed to be persuasive.

Applicant(s) argue that ...Iida fails to teach or suggest the step of causing the exchange of data between the host module and the memory device using at least one of the unused data lines.. (page 3). The Examiner does not agree. Iida teaches the use of unused data lines (DAT4-DAT7) to transfer data (i.e. exchange of data) between the host interface and the memory device when the level detection circuit 221 determines the high-speed 8-bit MMC mode or 4-bit MMC mode (i.e. data mode) (see para 44-48).

Applicant(s) argue that ...Moro teaching is to prevent the use of unused data line by using "the lead-through prevention function". (page 3). The Examiner does not agree. The lead-through current is caused when the data pin DAT1 and DAT2 of the SD card which are not used in the 1-bit mode (see para 9), therefore the use of lead-through current prevention is to stop the current between the power source terminal and the grounding terminal of the internal circuit (see para 9). Moro does not disclose or suggest the use of lead-through current prevention to prevent the use of unused data lines as stated by applicants.

Conclusion

6. All claims are rejected.

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 C.F.R. § 1.136(a).

A SHORTENED STATUTORY PERIOD FOR RESPONSE TO THIS FINAL ACTION IS SET TO EXPIRE THREE MONTHS FROM THE DATE OF THIS ACTION. IN THE EVENT A FIRST RESPONSE IS FILED WITHIN TWO MONTHS OF THE MAILING DATE OF THIS FINAL ACTION AND THE ADVISORY ACTION IS NOT MAILED UNTIL AFTER THE END OF THE THREE-MONTH SHORTENED STATUTORY PERIOD, THEN THE SHORTENED STATUTORY PERIOD WILL EXPIRE ON THE DATE THE ADVISORY ACTION IS MAILED, AND ANY EXTENSION FEE PURSUANT TO 37 C.F.R. § 1.136(a) WILL BE CALCULATED FROM THE MAILING DATE OF THE ADVISORY ACTION. IN NO EVENT WILL THE STATUTORY PERIOD FOR RESPONSE EXPIRE LATER THAN SIX MONTHS FROM THE DATE OF THIS FINAL ACTION.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Raymond Phan, whose telephone number is (571) 272-3630. The examiner can normally be reached on Monday-Friday from 6:30AM- 4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's Primary, Paul Myers can be reached on (571) 272-3639 or via e-mail addressed to paul.myers@uspto.gov. The fax phone number for this Group is (571) 273-8300.

Communications via Internet e-mail regarding this application, other than those under 35 U.S.C. 132 or which otherwise require a signature, may be used by the applicant and should be addressed to [**raymond.phan@uspto.gov**].

All Internet e-mail communications will be made of record in the application file. PTO employees do not engage in Internet communications where there exists a possibility that sensitive information could be identified or exchanged unless the record includes a properly signed express waiver of the confidentiality requirements of 35 U.S.C. 122. This is more clearly set forth in the Interim Internet Usage Policy published in the Official Gazette of the Patent and Trademark on February 25, 1997 at 1195 OG 89.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see hop://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 central telephone number is (571) 272-2100.

RP

Raymond Phan
April 3, 2006

JOHN R. COTTINGHAM
PRIMARY EXAMINER